IN THE SPECIFICATION:

Please amend the specification as follows:

Please replace the paragraph at page 1, lns. 4-9 with the following amended paragraph:

The present invention relates to a semiconductor nonvolatile memory particularly, a semiconductor nonvolatile memory in which writing and erasing can be electrically carried out (an electrically erasable and programmable read only memory referred to as EEPROM, hereinafter). The invention [[is]] also relates to a semiconductor device.

Please replace the paragraph at page 1, lns. 10-20 with the following amended paragraph:

An electrically erasable and programmable nonvolatile memory (EEPROM) is known as a memory representing semiconductor nonvolatile memories. An EEPROM is a nonvolatile memory and different from a DRAM (dynamic random access memory) and an SRAM (static RAM), which represent other semiconductor memories. Therefore, data in the EEPROM would not be lost even when a power source turns off. Further, the EEPROM has a characteristic superior in integration density, ballistic resistance, consumption power, and writing/reading speed, compared with a magnetic disc representing the nonvolatile memories other than the above EEPROM. Due to such characteristic, a trend using an EEPROM as a substitute for various memories such as a magnetic disc and a DRAM has been increased, and further development in the future is expected.

Please replace the paragraph at page 2, lns. 11-18 with the following amended paragraph:

A range for selecting a reading-out voltage is narrow when the dispersion width of a threshold voltage after writing or erasing is large. It is necessary to widen a space between

threshold voltages in respective storing conditions in order to accurately read out information, which ~~leads increase of~~ increases a writing time or an erasing time. Further, consumption power is also increased in writing or erasing. This is a further serious problem in a multi-value memory transistor in which three or more values of information are stored. Therefore, there has been an idea to decrease the dispersion width of a threshold voltage after writing or erasing.

Please replace the paragraph at page 2, lns. 19-30 with the following amended paragraph:

For example, manufacturing processes [[is]] are improved to manufacture a memory transistor having a uniform characteristic so that the dispersion width of a threshold voltage after writing or erasing can be decreased. This corresponds to make a difference small in writing speed between the memory transistor A in which a writing speed is fast and the memory transistor B in which a writing speed is slow, as shown in FIG. 2B. The threshold voltage after writing is distributed in the vicinity of a predetermined threshold voltage Vth when the writing time is set at t1. Dispersion width D1 of the threshold voltage after writing in this case is smaller than dispersion width D0 shown in FIG. 2A. In order to make a characteristic of a memory transistor uniform, there are so many points for improving the manufacturing processes that there is a limit in making the dispersion width of the threshold voltage small only by improving the manufacturing processes.

Please replace the paragraph at page 23, lns. 15-18 with the following amended paragraph:

A memory transistor according to the invention can be applied to various well-known circuit structures in which a nonvolatile storing element is used. In this embodiment, it will be described that the invention is applied to an NOR type of ~~flush~~ flash memory.

Please replace the paragraph at page 23, lns. 19-25 with the following amended paragraph:

FIG. 7A is a circuit diagram of an NOR type of ~~flush~~ flash memory circuit in which a memory transistor is arranged in a shape of matrix comprising m columns and n lines (m and n are respectively integers equal to or more than 1). A memory transistor in this embodiment is an N type memory transistor, which is described in the first mode and in which writing is self-concluded. That is, in each memory transistor, the threshold voltages in the writing region and the writing control-region are 0 V and 4 V, respectively, when no electric charge is accumulated in the floating gate.

Please replace the paragraph at page 24, lns. 4-6 with the following amended paragraph:

FIG. 7B shows an example of a top view of a memory transistor forming an NOR type of ~~flush~~ flash memory circuit shown in FIG. 7A. In FIG. 7B, a portion corresponding to that of FIG. 7A is marked with a same reference numeral.

Please replace the paragraph at page 24, lns. 10-14 with the following amended paragraph:

An operation of an NOR type of ~~flush~~ flash memory circuit comprising a memory transistor according to the invention as mentioned above will be now described. Writing is carried out by means of a hot electron, while erasing is carried out by means of the tunnel current flowing between the floating gate and the drain region. In the description, writing is carried out per a bit while erasing is carried out in the block.

Please replace the paragraph at page 25, ln. 31 - page 26, ln. 3 with the following amended paragraph:

FIG. 8 illustrates an example of a microprocessor. The microprocessor typically comprises a CPU core, a ~~flush~~ flash memory, a RAM, a clock controller, a cache memory, a cache controller, a serial interface and an I/O (input/output) port. The microprocessor shown in FIG. 7 is, of course, only a simplified example. A circuit of a microprocessor is variously designed in practice according to the usage thereof.

Please replace the paragraph at page 26, ln. 4-12 with the following amended paragraph:

In the microprocessor shown in FIG. 8, a CPU core 801, a cache memory 802, a clock controller 803, a cache controller 805, a serial interface 806 and an I/O port 807 are provided in a CMOS circuit. A memory transistor according to the invention is used for the ~~flush~~ flash memory 804. A nonvolatile memory comprising a memory transistor according to the invention may be used for the cache memory 802. The ~~flush~~ flash memory 804 and the cache memory 802 may be combined with any of structures in the first and second modes for carrying out the invention. A structure in this embodiment can be freely combined with any of structures in the Embodiments 1 to 3 to be put into practice.